3-D Technique Applied to Calculation Nodes, Pin to Pin Compatible with Embedded DSPs

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INTRODUCTION

Multichip Module technology (MCM's) has been traditionally used to support high performance microprocessor devices owning to this 2-D technique : excellent fine circuit routability, high frequency performances, lower volume and weight, and reliability. The driving forces behind 3-D packaging are the same as these behind 2D interconnection, but the vertical multichip module (MCM-V) enhances the performances.

MANUFACTURING TECHNIQUES

Three-dimensional packaging technique has been studied and developed for the Space, military, computer, and consumer electronic industries. More than 40 companies have patented, developed or manufactured 3-D modules. Among participating companies, the 3-D production status is at very different levels : research, development, characterization, qualification and production. 3D PLUS stacks any kind of components – memories, microprocessors, sensors, actuators, etc…This 3-D technique has been developed at Thomson-CSF from 1988 (9 patents are held in this area). On october 1995, three people launched a start-up – named 3-D Plus – to manufacture and commercialize these 3-D modules. A brief description of this technology is given.

3-D Plus / Thomson-CSF technique

This technique is used for bare die or packaged die

Bare die assembly

The 3-D technique is based on chip-on-tape - 35 mm. - making it possible to use the equipment dedicated to the manufacture of smart card and the tools realized for the TAB technique (sockets, etc...). After the electrical tests and eventual the burn-in, the tapes are stacked and molded with epoxy. At this step, machining by sawing (parallelepipedal bloc) or lathing (cylindrical bloc) allows a cross section of the leads to be printed on the tape (flex PCB). The entire module is metallized using a process similar to plating through-holes in printed circuit boards. The surface of the module is electroless deposited, then, copper, nickel and gold are electrochemically plated. The interconnect pattern on the surface of the cube or on the cylinder is generated by YAG laser trimming. A laser cuts the metal and gives a kerf that electrically isolates the conductors from the ground plane (see Figure 1). Generally, a lead frame (0.5 mm or 0.635 mm) is embedded in the module, the ball grid array technique can also be used. The third method is chip on board attachment .

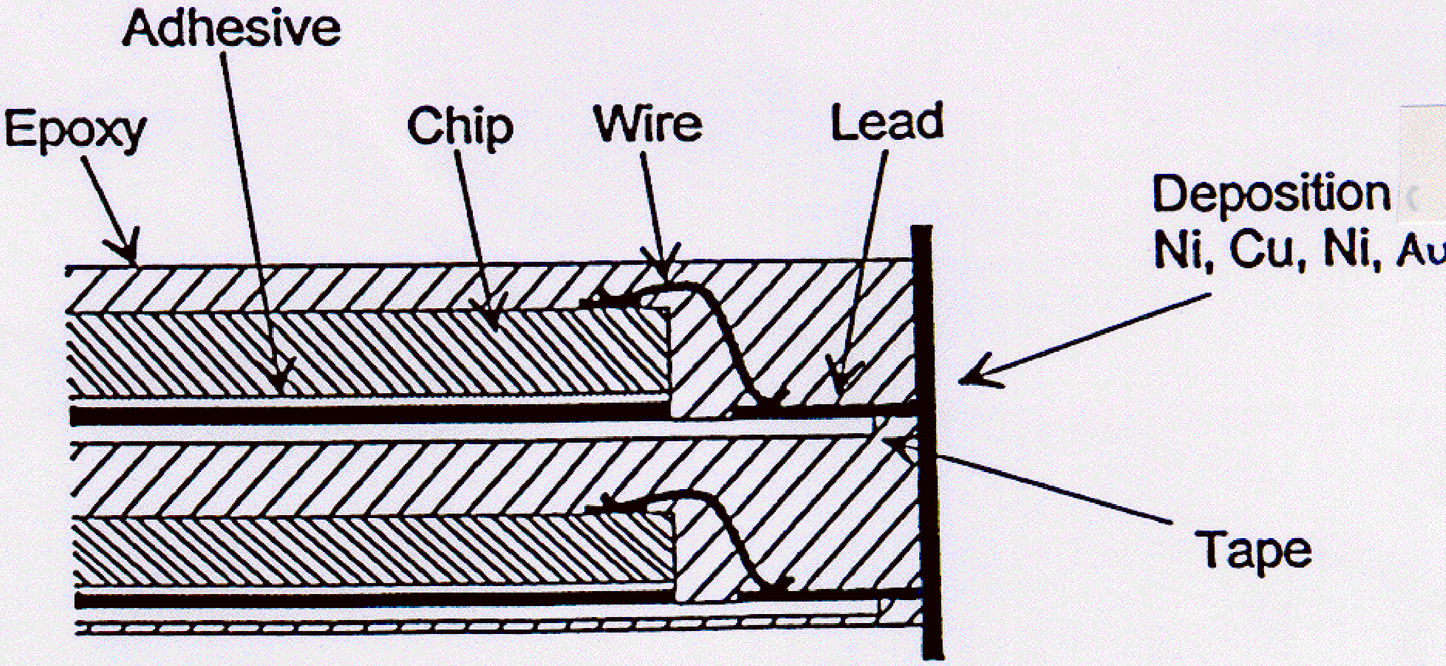


Figure 1 : 3-D Plus/Thomson-CSF technique.

Packaged die assembly

The standard TSOP – type I or II – or Chip-Scale-Package are surface mounted :

- on a thin printed circuit board like the bare die, for low power applications
- on copper lead frame, for high power applications (e.g. high speed SRAM).

Molding with a low expansion coefficient epoxy resin, then sawing, gives a part having a smaller area than the TSOP – the sawing is made at the level of the plastic body (see Figure. 2. An external connection level is stacked with the other levels of plastic packages in order to allow three kinds of external connection :

- Ball Grid Array,
- Gull wing,
- J-leads.

This external connections permit to fit the same foot print than standard Jedec package in order to upgrade an obsolete electronic function. The plating and the etching by Laser are exactly the same that those used for bare die.

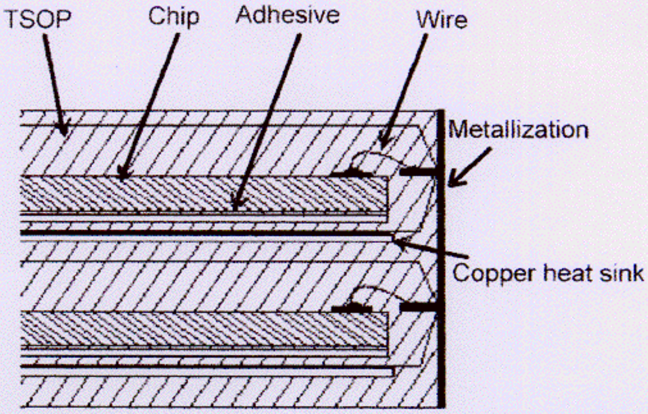


Figure 2 : 3-D Plus/Thomson-CSF method.

APPLICATIONS

The versatility of these 3D techniques permits to stack any kind of components from the identical devices (memory modules) to the heterogeneous components (calculation nodes, microcamera, microsystem).

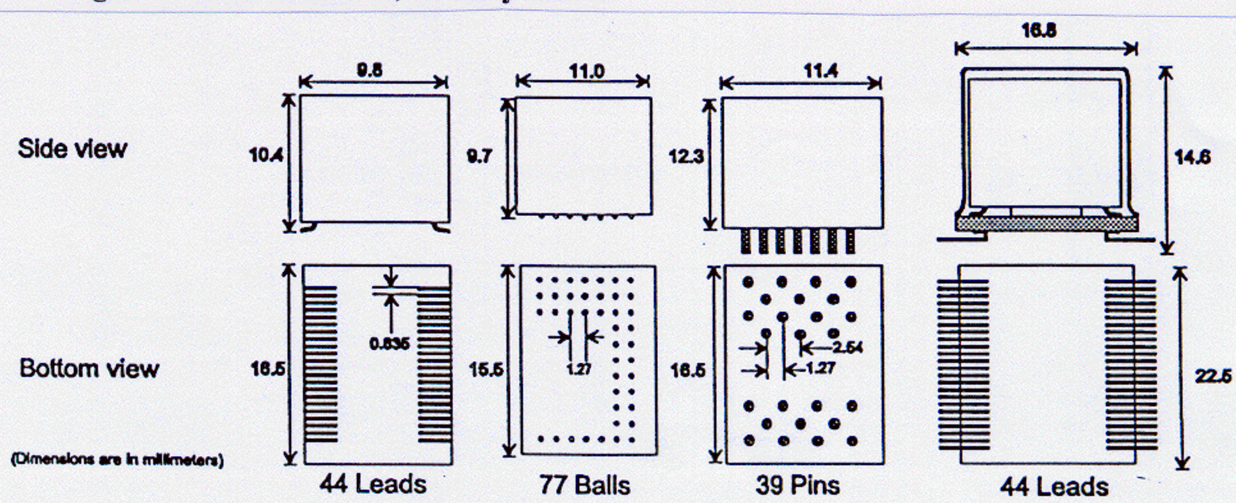
3D Modules with the same component/ Memory modules

A 128 Mbit DRAM requiring 8 memories 16Mbit LUNA ES3 wire bonded on a tape designed by 3D PLUS, tested and burned in by Montpellier Technology/IBM has been manufactured. Four kinds of external connection (see Figure 3) are available :

Surface mounting module with 2 x 22 leads (pitch of 0.635 mm),
Ball Grid Array with 77 balls (pitch of 1.27 mm),
Pin Grid Array for very high acceleration (20 to 30 000g for ammunition),
Wire bonded inside a hermetic ceramic package for military or space applications.

In this case, four blocks with 10 dice of 16Mbit DRAM LUNA ES4 from IBM, are mounted on a 84 "J" leads ceramic package in order to reach 640Mbit/package. These 640Mbit modules are used by DEMLER-BENZ/DASA/DORNIER for the European satellites "CLUSTER and ENVISAT. In the same way, four packaged die with plastic package are stacked. The use of 64Mbit DRAM in plastic package (TSOP) permits to get 256Mbit per block.

Figure 3 : 128 MB DRAM, Memory module



3D Modules with different kind of components/ Calculation nodes

- From 1992, calculation nodes for ammunition have been manufactured for Thomson-Daimler-Benz Armement, running after 20 000g in both direction (acceleration and deceleration).
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- From 1996, 3D PLUS has been awarded by the French Military Administration (DGA/DRET) an order for the prototyping of a computer recorder module. In this program, 3D PLUS is associated with GIAT Industries that designed the function. This module which dimensions are 30 x 30x 20 mm, is built around a DSP C31 from Texas Instruments. It is aimed to be embarked on ammunition whose caliber is between 155 mm and 45 mm.
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- More recently we developed a general purpose calculation node using a DSP C44 from Texas Instruments, with several generic levels :
    - Levels for 32Mbit SRAM (20 ns),
    - Level for 8Mbit FLASH,
    - Level for EPLD.
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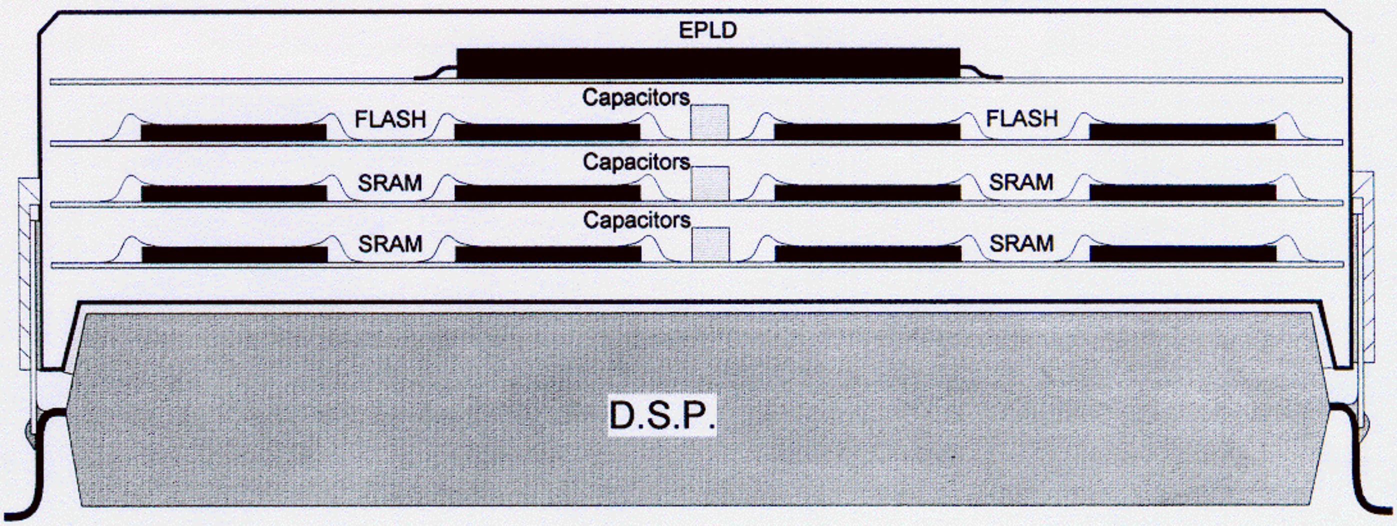
In order to reach a low price module, a packaged processor die (PQFP) is used instead of bare die. The problem was therefore : how to interconnect the 304 leads coming from the PQFP with the 3D block mounted above this PQFP. A very simple technique permits to interconnect the two parts. Thanks to that, the DSP can be upgraded with exactly the same footprint and pinout. The figure 4 shows a view of the calculation node, it can be seen that several packaged dice are used. The qualification of these modules are funded by the French Military Administration (DGA/DRET)

Nevertheless, fully bare dice calculation nodes based on an hardened microprocessor, are under development for space applications (funded by the ESA via CSEM).

Figure 4 : Calculation Node



Add-on components:
* SRAM - 1MBits 20ns (2 levels - 8 dice)
* FLASH - 4MBits (1 level - 4 dice)
* EPLD - EPM7128S (1 level - 1 TQFP100 package)

CONCLUSIONS AND PERSPECTIVES

The different applications, memory, calculation nodes, micro-cameras and microsystems will surely allow moving into smaller modules and for example, the smart pill with communication device, navigation system, etc seems reachable within 10 years. We can expect that the 3D techniques will permit to decrease the size of the microsystems from the centimetric to the millimetric range.

Recently , Mr G. W. La Rosa from IBM (Geneva) showed a roadmap for the future of the packaging where the ultimate concept was the 3D interconnection leading to a lot of functions like : the "Computing Package" Cube, the "Seeing Package" Cube and the "Hearing Package" Cube (see Figure 5).

Finally, the downsizing of the equipment opens the door of a lot of domains (space, defense equipments, telecommunication, medical, automotive,…), thanks to the cost reduction. It is common knowledge since the development of integrated circuits that it exists a close relationship between the cost of an equipment and its weight or volume.

So, the standardization of the 3D modules and microsystems will take time, but this way is very attractive.